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A FAULT-TOLERANT SENSORLESS APPROACH IN FIVE-LEVEL PACKED U CELLS (PUC5) MULTILEVEL INVERTER

Dhananjay Kumar,* Rajesh K. Nema,* Sushma Gupta,* and Niraj K. Dewangan*

Abstract

In this paper, a modified structure of fault-tolerant (FT) operation has been designed for the five-level packed U cells (PUC5) multilevel inverter (MLI). The sensorless self-capacitor voltage balancing control is designed to regulate the voltage across the capacitor at the half magnitude of the DC source value in creating a symmetrical five-level output voltage waveform. Moreover, the sensorless self-capacitor voltage balancing control reduces the complexity and improves the reliability of the system. Also, the proposed FT-PUC5 structure is considered and analysed for the open circuit (OC) fault in the switches. Based on a comparative analysis of the five-level PUC5 MLI and the proposed fault tolerance, the PUC MLI structure is presented. It has less number of devices in comparison with the most recent FT topologies. Moreover, this proposed single-phase and three-phase FT-PUC5 structure is established under before-fault, during-fault and after-fault operation using software MATLAB/Simulink. The proposed single-phase and three-phase FT-PUC5 structure is validated through an experimental prototype using the dSPACE DS-1104 real-time controller.

Key Words

Multilevel inverters (MLI), packed U cells (PUC), fault tolerance (FT), open circuit (OC), reliability

1. Introduction

Multilevel inverter (MLI) has numerous benefits over a classical two-level inverter in various industrial applications due to their high efficiency, low switching losses, less dv/dt stress and less total harmonic distortion (THD) [1], [2]. Numerous surveys have been published to introduce the three traditional MLI topologies including the cascaded H-bridge (CHB), flying capacitors (FC), and neutral-point clamped (NPC) converter [3]. Among traditional MLIs, one promising structure is the packed U cells (PUCs), which combines the benefits of the CHB and FC. The PUC MLI structure requires only one DC source. Similarly, the other needed sources are supplied by capacitors that act as auxiliary sources. [4], [5]. Unlike FC, the PUC structure produces the same level as the semiconductor device and half the voltage level of the capacitor. Moreover, the PUC inverter combines the FC and CHB. These advantages result in lower production cost, smaller sizes and highly compact power conversion units. The various control schemes have been studied about PUC such as non-linear controllers [6], [7] and hysteresis current control [8].

Researchers have been introducing lots of packed U cells (PUC) inverters topologies, which have been characterized by their less number of devices with high power quality and high flexibility in the multilevel voltage generation [9], [10]. The PUC inverter structure is based on hardware circuits proposed in [7], [8], [9], [11], and [12]. In [7] and [8], a model-predictive control (MPC) and finite control set (FCS) have been developed for the 7-level PUCs inverter in grid-connected application [9], [11]. However, FCS-MPCs not only suffer from variable and high switching frequency, but they are also highly dependent on converter models and component sizes. In [12] and [13], the operation with a single-phase 7-level PUC MLI control technique has been proposed for PV applications. However, the main disadvantage of the 7-level PUC MLI can be stated as the required complex controller to regulate charging and discharging the capacitor voltage, using a large capacitor. The hysteresis control technique of six bands for a 7-level PUC MLI was proposed in [14] and [15] in both rectifier and inverter modes. Moreover, the proposed hysteresis control is easily implemented, has high and variable switching frequencies, which increases the loss and can cause practical difficulties in filter design. A single-phase 5-level sensorless PUCs have been presented in [10], with the inherent capacitor voltage balanced also without the incorporation of an external controller and voltage feedback sensor [10]. However, all of these PUC topologies are applied to either stand-alone or grid-connected inverters. In these PUC topologies, although they have contained less number of power switches, any one of the power switch failures may cause overall system failure [9]–[15]. However, the concept of minimizing the number of power semiconductor switches or devices critically affected the reliability of the system.

* Electrical Engineering, Maulana Azad National Institute of Technology, Bhopal, India; e-mail: {dhananjaymanit23, nirajdewangan11}@gmail.com, {rk_nema, sush_gupta}@yahoo.com
Corresponding author: Dhananjay Kumar
Recommended by Prof. Ikhlaq Hussain
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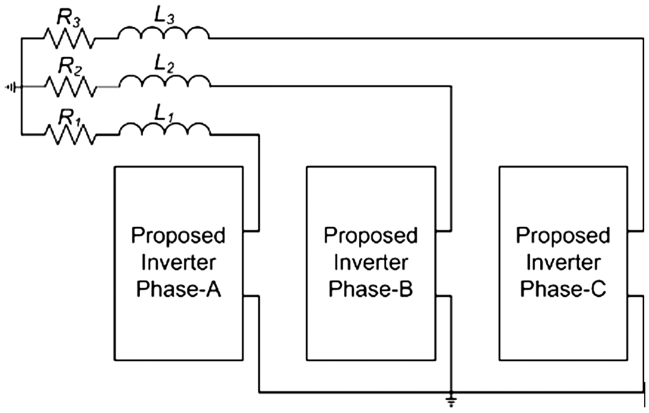


Figure 1. Schematic diagram of three-phase five-level PUC5 MLI structure.

Power devices are comparatively vulnerable, limiting system reliability [16]. Faults in electrical power devices can be categorized into short-circuit (SC) faults and open-circuit (OC) faults. Basically, the SC faults are severe faults that are difficult to handle and cause serious damage to other parts. Faulted parts in the SC state must be dismantled from the system immediately [17]–[20].

The content of this paper is structured as follows: Section 2 focuses on the operating principle of the PUC MLI structure along with OC FC techniques. Section 3 presents a power loss and efficiency analysis of the proposed FT-PUC5 MLI structure. The control method and MATLAB/Simulink results are described in Section 4. The experimental validation of the proposed FT-PUC5 MLI structure is proposed in Section 5. A comparative analysis of and the feasibility of the proposed FT PUC5 structure have been presented in Section 6. Finally, the conclusive analysis is presented in Section 7.

2. Operating Principle of the Proposed PUC MLI Structure

2.1 Analysis of OC Faults in 5-level PUC Inverter

A schematic diagram of the three-phase PUC5 MLI structure is shown in Fig. 1, and Phase-A of the proposed PUC structure is shown in Fig. 2. The proposed PUC5 (5-level) MLI consists of six unidirectional switches (S_1 to S_6) per phase that include one DC source voltage (V_1) and a self-voltage balancing capacitor. Different switching configurations (S_1, S_4), (S_2, S_5) and (S_3, S_6) are controlled in a complementary scheme. The eight switching state configurations of PUC5, named as σ_i ($i = 0, 1, 2, 3, 4, 5, 6, 7$), are listed in Table 1.

Table 2 presents the availability of operating status. To realize the PUC5 MLI for the case of anyone of the switches (S_2, S_3, S_5 and S_6) undergoing an OC fault, the structure can continue to operate with a three-level output voltage. On the other hand, if any one of the switches S_1, S_4 undergoes an OC fault, then the available state will not allow the generation of alternating MLI output voltage levels.

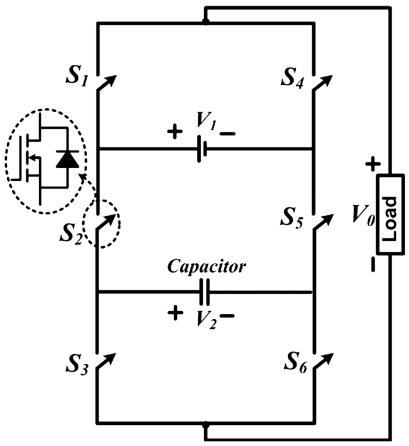


Figure 2. Phase-A of proposed five-level PUC5 MLI structure [10].

Table 1
Possible Switching State of the Studied PUC5 (5-level) MLI

State	Switching Number	Output Voltage Magnitude	Output Level per Phase	Effect on Capacitor
σ_0	S_1, S_5, S_6	$+V_1$	$+2E$	Bypassed
σ_1	S_1, S_3, S_5	$+V_1 - V_2$	$+E$	Charged
σ_2	S_1, S_2, S_6	$+V_2$	$+E$	Discharged
σ_3	S_1, S_2, S_3	0	0	Bypassed
σ_4	S_4, S_5, S_6	0	0	Bypassed
σ_5	S_3, S_4, S_5	$-V_2$	$-E$	Charged
σ_6	S_2, S_4, S_6	$V_2 - V_1$	$-E$	Discharged
σ_7	S_2, S_3, S_4	$-V_1$	$-2E$	Bypassed

Table 2
Available States in Case of Any Single Switch OC Fault in PUC5 MLI

Failed Switch	Available States	Operation
S_1	σ_4, σ_5, σ_6, σ_7	Shut-down
S_2	σ_0, σ_1, σ_4, σ_5	Three-level
S_3	σ_0, σ_2, σ_4, σ_6	Three-level
S_4	σ_0, σ_1, σ_2, σ_3	Shut-down
S_5	σ_2, σ_3, σ_6, σ_7	Three-level
S_6	σ_1, σ_3, σ_5, σ_7	Three-level

For better understanding, Fig. 3 represents a complete cycle of the 5-level output voltage and current waveform. The self-voltage-balancing process based on the capacitor power relationship is mathematically proved.

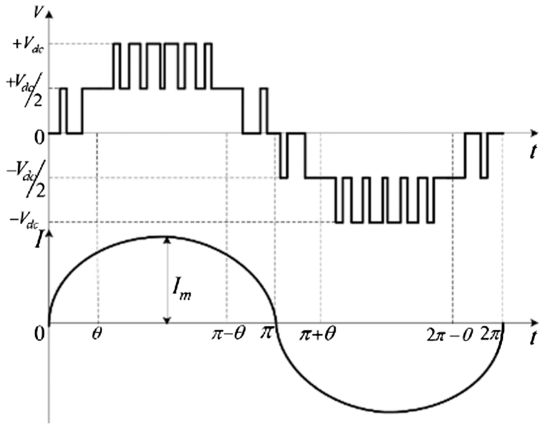


Figure 3. Complete cycle of the five-level output voltage and current waveform.

Let us assume that $V(x)$ represents fundamental voltage

$$V(x) = V_m \sin(\omega t) \tag{1}$$

Let us assume that instantaneous current $(I)$is

$$I = I_m \sin(\omega t - \phi) \tag{2}$$

Where V_m and I_m represent the maximum value of output voltage and load current waveforms, respectively; also ϕ represents the power factor angle.

The energy transferred to the load$(E)$by the DC capacitor can be shown as follows:

The energy transferred (E) to the load by DC capacitor can be expressed as

$$I = \frac{dq}{dt} \tag{3}$$
$$dE = Vdq = V * I * dt$$

Where I and q represent the instantaneous current and electric charge, respectively

$$E = \int V * I * dt$$

For evaluating capacitor energy in positive half-voltage level equation can be expressed in the following:

$$E^+ = \int_0^{\Pi} V_K * I * dt \tag{4}$$
$$E^+ = \int_0^{\Pi} V_K I_m \sin(\omega t - \phi) d(\omega t)$$
$$\therefore E^+ = I_m \int_0^{\Pi} V_K \sin(\omega t - \phi) d(\omega t)$$
$$= -VI_m \cos(\omega t - \phi) \Big|_{\theta_1}^{\theta_2} - VI_m \cos(\omega t - \phi) \Big|_{\theta_3}^{\theta_4}$$
$$= VI_m \begin{bmatrix} \cos(\theta_1 - \phi) - \cos(\theta_2 - \phi) \\ +\cos(\theta_3 - \phi) - \cos(\theta_4 - \phi) \end{bmatrix} \tag{5}$$

For calculating capacitor energy in negative half-voltage level equation can be shown in the following:

$$E^- = \int_0^{2\Pi} V_K I_m \sin(\omega t - \phi) d(\omega t) \tag{6}$$
$$\therefore E^- = I_m \int_{\Pi}^{2\Pi} V_K \sin(\omega t - \phi) d(\omega t)$$
$$= -VI_m \cos(\omega t - \phi) \Big|_{\theta_5}^{\theta_6} - VI_m \cos(\omega t - \phi) \Big|_{\theta_7}^{\theta_8}$$
$$= VI_m \begin{bmatrix} \cos((\Pi + \theta_2) - \phi) - \cos((\Pi + \theta_1) - \phi)) \\ +\cos((\Pi + \theta_4) - \phi) - \cos((\Pi + \theta_3) - \phi) \end{bmatrix} \tag{7}$$

From (5) and (7), it can be indicated that in the half-cycle the amount of energy would be opposite in sign but equal in value.

Table 2 shows that if any one of the switches S_2, S_3, S_5 and S_6 encounters a failure. The output voltage is reduced from five-level to three-level with reduction of voltage magnitude to one half of the peak.

2.2 Design of Proposed Fault-Tolerant PUC Inverter Structure

The conventional topology requires the FT feature obstructing the output for faults in the switches. The authors have addressed the issue and some modifications in the existing single-phase PUC5 MLI to incorporate inherent FT capability. Additional switches S_7 and S_8 have been added to the conventional PUC5 MLI, to obtain the modified single-phase PUC5 (5-level) MLI with FT feature as shown in Fig. 4.

The valid switching status of the proposed FT-PUC5 MLI in case of single switch faulty conditions is presented in Table 3.

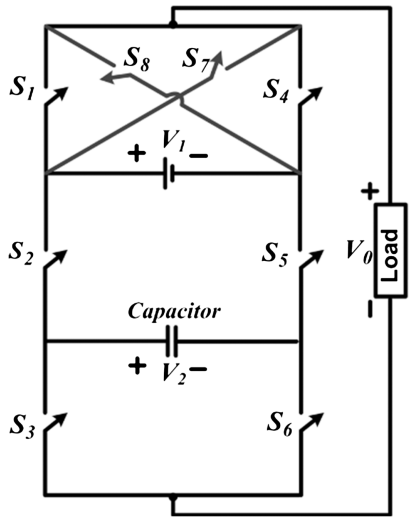


Figure 4. The Proposed FT-PUC5 MLI structure.

Table 3
Available Output Voltage Levels of the Proposed FT-PUC5 MLI in Case of Single Switch Failure

Failed Switch	Magnitude					Operation Level
	$+2E$	$+E$	0	$-E$	$-2E$	
S_1	✓	✓	✓	✓	✓	Five-Level
S_2	×	✓	✓	✓	×	Three-Level
S_3	×	✓	✓	✓	×	Three-Level
S_4	✓	✓	✓	✓	✓	Five Level
S_5	×	✓	✓	✓	×	Three-Level
S_6	×	✓	✓	✓	×	Three-Level
S_7	✓	✓	✓	✓	✓	Five-Level
S_8	✓	✓	✓	✓	✓	Five-Level

3. Power Loss and Efficiency Analysis

Basically, two types of losses, conduction and switching losses, are associated with power semiconductor devices (MOSFET and Diode) as used in the proposed PUC5 MLI structure. The conduction power losses (P_C) occur due to the flow of current in power semiconductor devices during ON-state voltage. For this purpose, load current in a power semiconductor devices flows through the MOSFET and anti-parallel diode in MLI. Therefore, the conduction power losses of a MOSFET ($P_{C,MOSFET}$) and diode ($P_{C,Diode}$) can be written as follows:

$$P_{C,MOSFET} = n_{MOSFET}(t) \times \left[\frac{1}{2\prod}\int_0^{2\Pi}\left[V_{ON,MOSFET}I + R_{ON,MOSFET}I^{\beta+1}d(\omega t)\right]\right] \tag{8}$$

$$P_{C,Diode} = n_{Diode}(t) \times \left[\frac{1}{2\prod}\int_0^{2\Pi}\left[V_{ON,Diode} + R_{ON,Diode}I^2 d(\omega t)\right]\right] \tag{9}$$

$$P_C = P_{C,MOSFET} + P_{C,Diode} \tag{10}$$

Where $n_{MOSFET}(t)$ and $n_{Diode}(t)$ are the ON-state voltage of the MOSFET and anti-parallel diode, respectively. $R_{ON,MOSFET}$ and $R_{ON,Diode}$ are the equivalent resistance of the MOSFET and anti-parallel diode, respectively, and β is a constant related to the specification of the MOSFET. Switching loss (P_S) is dissipated power during the turning on and the turning off. Turning-on and turning-off energy loss ($E_{on,T}$, $E_{off,T}$) of a power switch can be evaluated as:

$$\begin{aligned} E_{on,T} &= \int_0^{ton} v(t)i(t)dt \\ &= \int_0^{ton}\left[\left(\frac{V_{sw}t}{t_{off}}\right)\left(-\frac{I_1(t-t_{on})}{t_{on}}\right)\right]dt \\ &= \frac{1}{6}V_{SW}I_1 t_{on} \end{aligned} \tag{11}$$

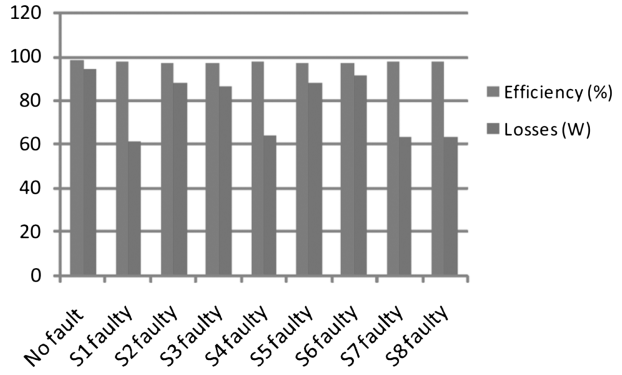


Figure 5. Efficiency and power losses of the proposed PUC5 structure.

$$\begin{aligned} E_{off,T} &= \int_0^{t\,off} v(t)i(t)dt \\ &= \int_0^{t\,off}\left[\left(\frac{V_{sw}t}{t_{off}}\right)\left(-\frac{I_2(t-t_{off})}{t_{off}}\right)\right]dt \\ &= \frac{1}{6}V_{SW}I_2 t_{off} \end{aligned} \tag{12}$$

This equation, $E_{on,T}$ and $E_{off,T}$, represents the energy losses for the turning-on and turning-off time period of the switch (MOSFET), t_{on} and t_{off} are the turning-on and turning-off cross-over interval time of the switch (MOSFET). The switching power loss of the switch (P_S) can be expressed as:

$$P_S = \frac{1}{T}\left(N_{on}E_{on} + N_{off}E_{off}\right) \tag{13}$$

Therefore, total power loss of the proposed MLI PUC5 MLI is calculated as:

$$P_{loss} = P_{C,MOSFET} + P_{C,Diode} + P_S \tag{14}$$

By using these equations, the total power loss of the proposed PUC5 MLI structure can be evaluated. In addition, the efficiency (η) can be evaluated as follows:

$$\eta = \frac{P_{out}}{P_{in}} = \frac{P_{out}}{P_{out} + P_{loss}} \tag{15}$$

The power loss and efficiency quantitatively analysis is carried out based on the above equation [19]. IRF640NSTRLPBF MOSFET switches are used to evaluate the efficiency and power loss of the proposed MLI structure, and the following parameters are considered: input voltage $V_S = 96$ V, RL load ($R = 20\Omega$, $L = 20$ mH). Figure 5 shows the efficiency and power loss of the proposed 5-level MLI structure under healthy (no fault) conditions and in case of any single switch OC faulty conditions.

The efficiency and power loss analysis graph of the proposed PUC5 structure has been carried out in both healthy (no fault) and faulty conditions using the (16)–(23). In this paper, under any single switch failure condition, the number of levels in the output voltage waveform remains the same or reduced. Also, the proposed PUC5 MLI with added switches configuration is more efficient and reliable than the used configuration. Hence, a better understanding

Table 4
Failure Rate of Switches and Capacitor in the Proposed PUC5 MLI Structure

Component Voltage	S1	S2	S3	S4	S5	S6	S7	S8	Cap(C)
stress factor ($V_{S,S}$)	0.0625	0.125	0.125	0.0625	0.125	0.125	0.0625	0.0625	0.125
Power loss, W (P_{Switch})	1.93	1.21	1.05	1.92	1.24	1.05	0.72	0.72	N/A
Failure rate, (λ_S)	0.0037	0.0045	0.0018	0.0037	0.0045	0.0045	0.0018	0.0027	0.002

Table 5
Simulation and Experimental Parameters

Components	Rating
Rated DC voltage (lead acid battery)	$V_S = 96\ V$
Capacitor (LGU2A222MELA)	$C_1 = 2{,}500\mu F$
MOSFET switch (IRF640NSTRLPBF)	1200V, 30A
Modulation index	$m_a = 0.85$
Switching frequency	$f_s = 2{,}000$ kHz
Controller	dSPACE-1104
Gate driver	M57962L
Load	$R = 20\Omega$, $L = 20$ mH

of calculated power loss and failure rate across the switches and capacitor in the proposed PUC5 MLI structure is presented in Table 4.

4. Simulation Results

In this section, the results of simulation studies of the proposed FT-PUC5 structure are described. The proposed FT-PUC5 is simulated using MATLAB/Simulink software to verify the structure under before-fault, faulty and after-fault conditions. In the present work, the multicarrier phase opposition disposition PWM (POD-PWM) scheme with level shifting (LS-PWM) is adopted. The LS-PWM modulation is used to generate gate pulses for triggering ON the power switching devices [20].

The simulation and experimental parameters for both the proposed FT-PUC5 structure are shown in Table 5.

Figures 6 and 7 show the output voltage and load current waveforms for OC fault in switches S_2 and S_4, respectively. The output waveform are maintained due to the redundant paths available for these faults

Similar results are obtained in the case of the three-phase structure of the proposed PUC5 MLI. Figure 8 shows the phase voltages of the proposed FT-PUC5 MLI structure for an OC fault in the switch S_1. Figure 8(b) and (c) show the line-to-line voltages and load current, respectively.

Notably, the result clearly presented that the proposed FT-PUC5 structure has the FT feature against OC faults, that is, any single switch failure. The output voltage is reduced from five-level to three-level and peak magnitude is halved. Simultaneously, a similar effect shows on the load current.

5. Experimental Results

A laboratory prototype has been developed experimentally to verify the representation of the proposed FT-PUC (FT 5-level) structure. Control signals for discrete power circuit switching pulses are produced from dSPACE DS-1104 as a real-time controller. It is an interface with that MATLAB/Simulink model in the host PC. Figure 9 shows a laboratory prototype experimental setup. All the experimental results are recorded and measured with the help of a scopecorder YOKOGAWA DL750E.

The experimental results for the FT-PUC5 proposed 5-level output voltage of 96V peak to peak and 60.8V RMS prototype MLI output at the frequency of 50Hz are shown in Fig. 10(a) before OC fault condition. Similarly, experimental results for three-phase fault in switch S_1 for proposed FT-PUC MLI structure is shown in Fig. 11. The voltage THD obtained is 7.8% and 1.4% the current THD as shown in Fig. 12(a) and (b), respectively. The power quality analyser (FLUKE 43B) measures experimental THD, mainly up to the 49th order harmonics.

6. Comparative Analysis

In this section, the required parameters have been compared in the topology and in terms of advantages and limitations. In Table 6, the proposed FT-PUC5 MLI structure has been compared with existing recently published five-level MLI topologies. In terms of essential parameters such as number of DC source, capacitor, diodes, switches, drivers, reliability and FT ability have been investigated. A detailed comparison with the conventional topologies

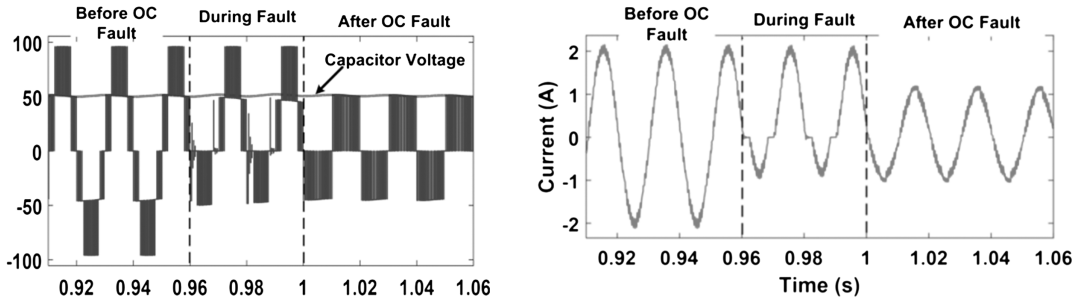


Figure 6. Simulation voltage and load current waveform under S_2 fault.

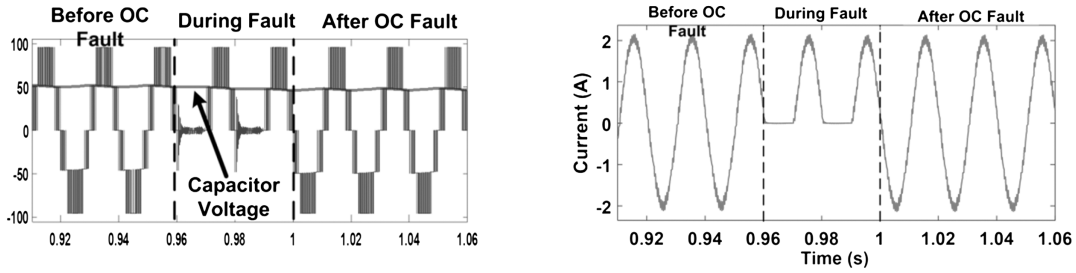


Figure 7. Simulation voltage and load current waveform under S_4 fault.

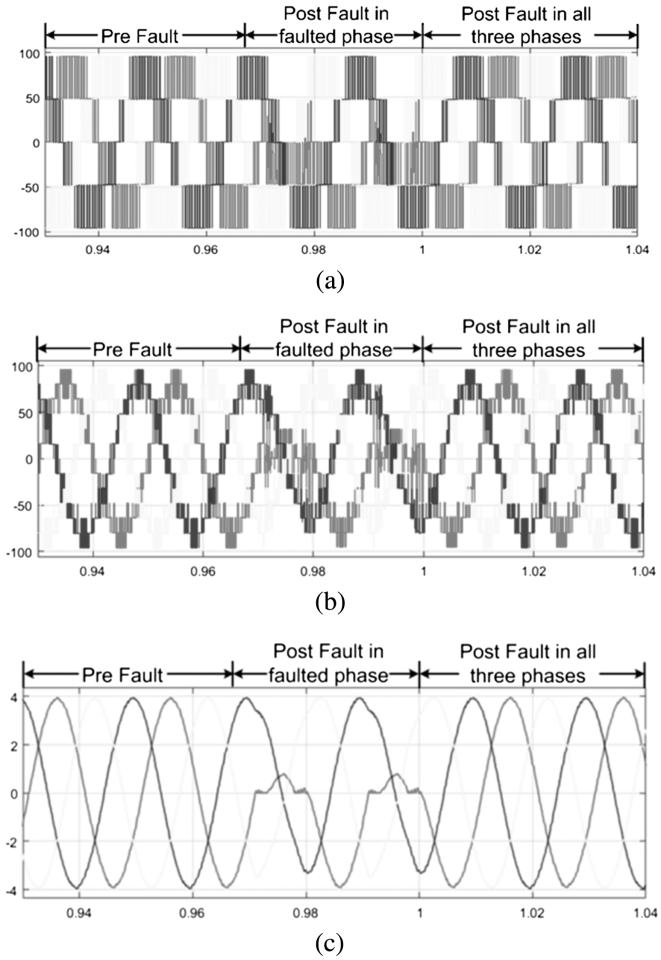


Figure 8. Simulation results for the proposed FT-PUC5 structure in switch S_1 under pre-fault, faulty, post-fault states, (a) Line voltages; (b) phase voltages; and (c) phase currents.

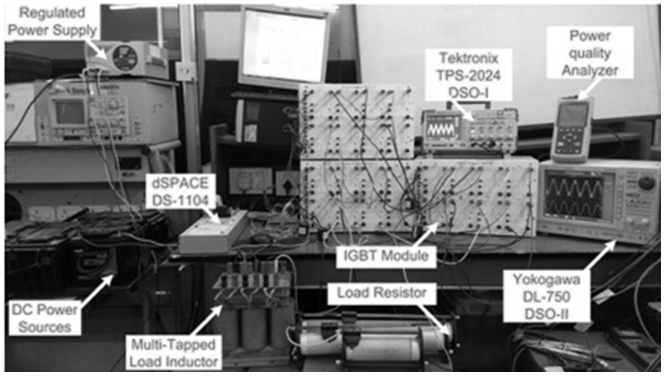


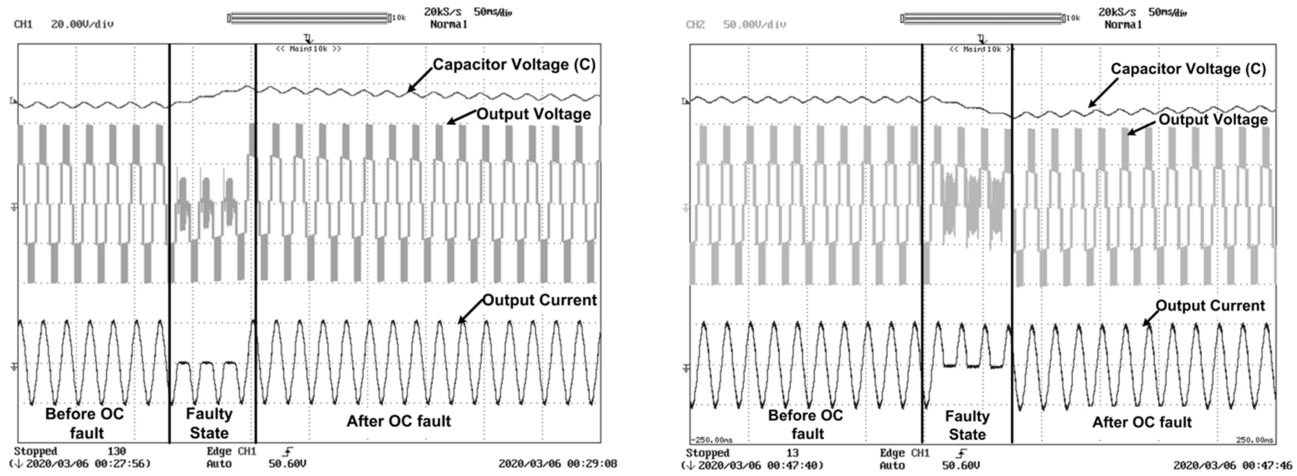
Figure 9. Experimental set-up of the proposed FT-PUC5 MLI.

and the topologies proposed in [16]–[20] is considered to produce a 5-level voltage.

The proposed FT-PUC5 structure is also compared for its reliability and FT ability. Also, the proposed FT-PUC5 MLI structure proves the merits of reduced device counts over the existing topologies.

7. Conclusion

This paper has presented a single-phase FT-PUC5 MLI structure with multiple redundant levels to overcome OC fault in switches with a reduced device count. Also, the proposed FT-PUC5 sensorless modulation technique has been estimated for all before-fault, faulty and after-fault modes. Furthermore, the proposed sensorless PWM scheme has self-balancing of the FT-PUC5 capacitor voltage and does not need complex calculations or extra hardware. The failure rate of the switches and capacitors has been calculated with consideration of power loss. It preserves the



(a) Fault in S_1 (b) Fault in S_4

Figure 10. Experimental results of capacitor voltage (50V/div), output voltage (50V/div) and load current (2A/div) for the proposed single-phase FT-PUC5 MLI structure across S_1 (a) fault in (b) fault in S_4.

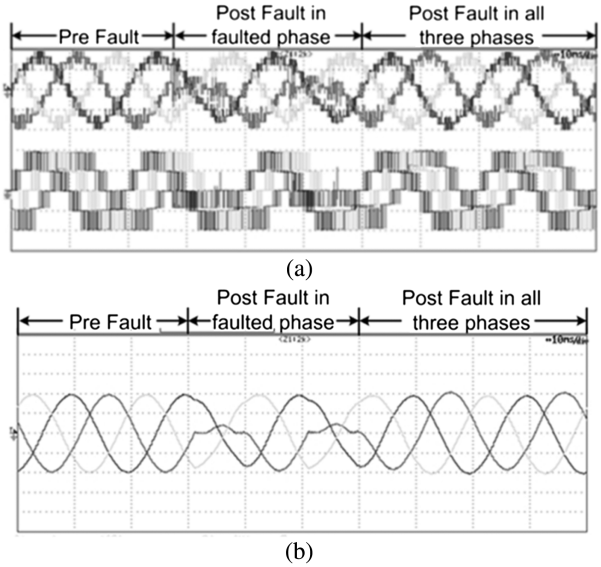
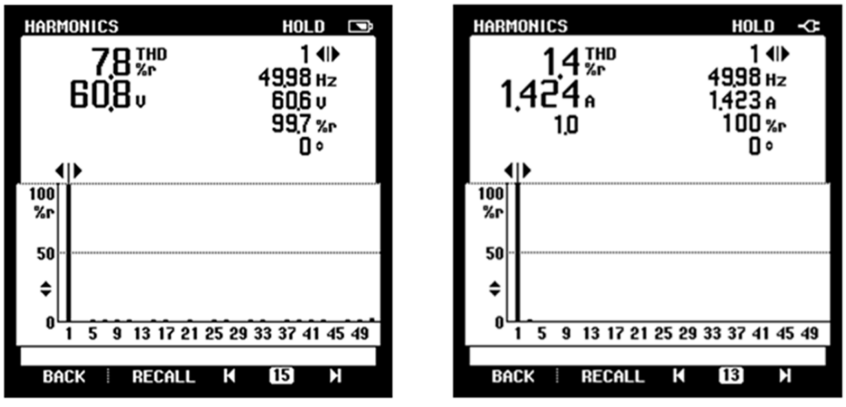


Figure 11. Experimental output for three-phase fault in switch S_1; (a) phase voltages (50V/div) and line voltages (50V/div), (b) phase currents (2A/div).



(a) (b)

Figure 12. THD result under healthy condition. (a) Voltage harmonic spectrum and (b) current harmonic spectrum.

Table 6
Comparison of the Topology Parameters with Recently Published Five-Level MLIs

MLI Structure Type	DC Sources	Capacitors	Main Diodes	Power Switches	Reliability	Output Voltage
NPCMLI	4	0	12	8	No	5
FCMLI	4	6	0	8	No	5
CHBMLI	2	0	0	8	Yes	5
[16]	1	8	0	22	Yes	5
[17]	4	0	0	20	Yes	5
[18]	2	0	2	8	Yes	5
[19]	1	2	2	8	Yes	5
[20]	2	0	0	8	Yes	5
Proposed FT-PUC5 structure	1	1	0	8	Yes	5

output power, voltage level and capacitor voltage balance before and after the OC fault operation. The comparative analysis incorporates a less number of devices to the proposed FT-PUC5 structure than the recently developed FT topologies. Finally, several simulation and experimental results prove that suitable fault tolerance of the proposed PUC5 MLI structure by considering THD value.

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Biographies

Dhananjay Kumar was born in Ballia, India, in 1992. He received his BE degree from Lakshmi Narain College of Technology, Bhopal, India, in 2014. In the year 2017, he received M.Tech degree from Maulana Azad National Institute of Technology (MANIT), Bhopal, India. Currently, he is pursuing his Ph.D. at MANIT Bhopal, India. He has published over 10+ articles/papers in various referred national/international conferences and journals and is serving as a reviewer of several journals. His main research interests include power electronic converter topologies and reliability aspects of power converters.

Rajesh K. Nema received his B.Tech and M.Tech degrees in Electrical engineering from Bhopal University in 1986 and 1992, respectively. He obtained Ph.D. degree in Electrical engineering from Barkatullah University, Bhopal, in 2004. From 2010, he has been working as professor in Electrical Engineering Department, MANIT Bhopal. He is the author of more than 150 articles. His current research interests include multilevel Inverter, solar PV controller and power electronics converter for renewable energy applications.

Sushma Gupta received the B.E. and M.E. degrees from Barakatullah University, Bhopal, India, in 1993 and 1999, respectively. She received her Ph.D. degree from Indian Institute of Technology, Delhi. She was a lecturer in the Electronic Engineering Department, Government Engineering College, Rewa, India, from 1994 to 1997. Currently, she is working as professor in Electrical Engineering Department, MANIT Bhopal. India. Her main research interests are power electronics, machines, digital electronics and self-excited induction generator.

Niraj K. Dewangan was born in India in 1986. He received B.Tech degree in Electronics and Telecommunication from B.P.U.T, Odisha, in 2008 and M.Tech degree in Digital Communication from R.G.P.V, Bhopal, in 2014. He obtained Ph.D. degree in Department of Electrical Engineering, National Institute of Technology, Raipur, in 2020. Currently, he is working as an assistant professor at the Dept. of Electrical engineering in NIT Raipur. He has published over 15+ articles/papers in various referred national/international conferences and journals and is serving as a reviewer of several journals (IET PE, IEEE PE, Wiley ITEES). His research fields of interest are multilevel inverters, fault tolerance in multilevel inverters, reduced device count MLIs, power electronics for renewable energy, real-time controllers for power electronic systems and modulation strategies for power converters.