International Journal of Power and Energy Systems, Vol. 43, No. 10, 2023
An open access paper

FIVE-LEVEL CASCADED H-BRIDGE MLI USING NEW IN-PHASE DISPOSITION PWM TECHNIQUE FOR HARMONICS MITIGATION

Vishal Rathore* and K. B. Yadav*

Abstract

In recent years, multi-phase multilevel inverters (MLIs) with different topologies have been used in various drives due to the potential benefits of multi-phase, over three-phase, in industrial applications. In this paper, performance analysis of five-level cascaded H-bridge multilevel inverter (CHB-MLI) using a new in-phase disposition (IPD) multicarrier pulse width modulation (PWM) technique for harmonic mitigation is presented. In the proposed work, MLI is also implemented with phase disposition (PD), phase opposition disposition (POD), and alternate phase opposition disposition (APOD) PWM techniques. The Matlab/Simulink platform is used to model the proposed topologies. Results obtained from the simulation are compared with the proposed IPD topology. The analysis of results shows that the proposed topology mitigates the current and voltage harmonics to 1.7% and 6.15% and increases the system's efficiency with reduced power loss. Finally, the system efficacy is validated by the real-time digital simulator Opal-RT OP4500.

Key Words

H-bridge MLI, In-phase disposition, pulse width modulation, Opal-RT OP4500.

1. Introduction

Nowadays, most medium- and high-power variable speed drives use multi-phase machines instead of three-phase machines due to their high torque density, high reliability, enhanced modularity, and greater efficiency [1, 2]. Development in multi-phase drives is initiated by their potential applications in the ship propulsion system, hybrid electric vehicles, aircraft, traction drive, and other high-power industrial applications. This leads to the development of pulse width modulation (PWM)-based multilevel inverters (MLIs) [3, 4], which reduces the requirement of a bulky transformer. MLI with a suitable PWM technique has been admitted as a feasible solution to overcome the voltage and current harmonics of the switching converters in high-power drive applications [5, 6]. When applied to an induction machine, PWM techniques reduce the torque pulsation and improve the efficiency of the MLI by controlling the harmonics of the output voltage and current [7, 8]. Based on the alignment of different carrier signals, PWM techniques for MLIs is of three types phase disposition (PD), phase opposition disposition (POD), and alternate phase opposition disposition (APOD). A comparative analysis of different PWM techniques using a seven-level inverter is presented in [9], and for a nine-level inverter is in [10].

Moreover, the harmonics can be further reduced by changing one carrier signal's phase shift in PD topology. A nine-level inverter using a similar topology with induction motor as a load is presented in [11]. The potential advantage of using MLI is its stepped output voltage which reduces the requirement of the bulky distribution transformer at the consumers level, thereby reducing the cost of transmission system employed for high-frequency, high-power industrial applications. The MLIs are mainly classified into three topologies: diode clamped, capacitor clamped, and cascaded [12]. Cascaded MLI is more common among the various topologies because of its higher output voltage. It does not require extra components like diode and capacitor, which increases the degree of freedom and provides a flexible structure with increased power levels [13].

MLI on combining with multi-phase machine results in a new arrangement of power segmentation with various potential benefits of both designs. A dual stator induction motor (DSIM) has the edge over other multi-phase motors, *i.e.*, it cancels out the pulsating even harmonic torque components from the individual stator due to opposition when the stator set is supplied from a six-phase inverter and also mitigates the odd harmonics component. Furthermore, DSIM requires less coil insulation and offers low stator resistance and leakage reactance than its three-phase counterparts, reducing the capability to restrain the stator harmonic currents [14, 15]. Also, the newly developed model allows the adaptation of volts/hertz control [16] and different modulation techniques to mitigate the harmonics and torque ripple with soft switching of the inverter switches [17]. This paper aims to compare the perfor-

* National Institute of Technology Jamshedpur, Jamshedpur 831014, India; e-mail: vishalrathore01@gmail.com, kbyadav.ee@nitjsr.ac.in
Corresponding author: Vishal Rathore
Recommended by: Rouhollah Shafaei
(DOI: 10.2316/J.2023.203-0345)

mance of a new IPD topology based on cascaded H-bridge multilevel inverter (CHB-MLI) with different multicarrier PWM topologies used to drive DSIM based on total harmonic distortion (THD), efficiency, and power loss. OPAL-RT (OP4500) is used to verify the correctness of the proposed scheme.

2. Cascaded H-bridge Multilevel Inverter

CHB-MLI is commonly used for industrial drives applications due to its ability to supply high-power output, eliminating the need for coupling a transformer to an interface with a common point of connection to the distribution network [18]. CHB-MLI topology consists of serially connected several H-bridge cells, as shown in Fig. 1. A separate DC source is required to supply each cell to generate square wave outputs, which are the cumulative output voltage of H-bridge cells [19].

The generalized output phase voltage is represented as:

$$V_0(t) = V_{01}(t) + V_{02}(t) + V_{03}(t) + V_{0N}(t) \tag{1}$$

where N represents the number of H-bridge cell connected in cascade.

The output voltage of the inverter *Vo(t)* is determined from each cell of the H-bridge switching state as:

$$V_0(t) = \sum_{j-1}^{n} (p_j - 1) \cdot V_{0N \cdot j} \qquad \text{where, } p_j = 0, 1, \tag{2}$$

The corresponding wave has the Fourier transform as [14]:

$$V(wt) = \frac{4V_{dc}}{\pi} \tag{3}$$
$$\sum_m [\cos m\theta_1 + \cos m\theta_2 + \cos m\theta_3 + \cos m\theta_i] \frac{\sin(m\omega t)}{m}$$

The magnitudes of the Fourier coefficient when normalized to V_{dc} as follows:

$$H(m) = \frac{4V_{dc}}{\pi} \tag{4}$$
$$\sum_m [\cos m\theta_1 + \cos m\theta_2 + \cos m\theta_3 + \cos m\theta_i] \frac{\sin(m\omega t)}{m}$$

2.1 Multicarrier PWM Techniques

The multicarrier level-shifted PWM scheme for cascaded H-bridge inverters requires (n-1) triangular carriers. All carrier waves are disposed of vertically to occupy a contiguous band. The multicarrier level-shifted PWM scheme with different phase relations are as follows:

- PD: The (n-1) triangular carrier signals are in the same phase.
- POD: For this technique, carrier signals below and above the reference zero are 180 degrees out of phase.
- APOD: In this case, each carrier signal is in 180-degree phase opposition with its adjacent carrier.

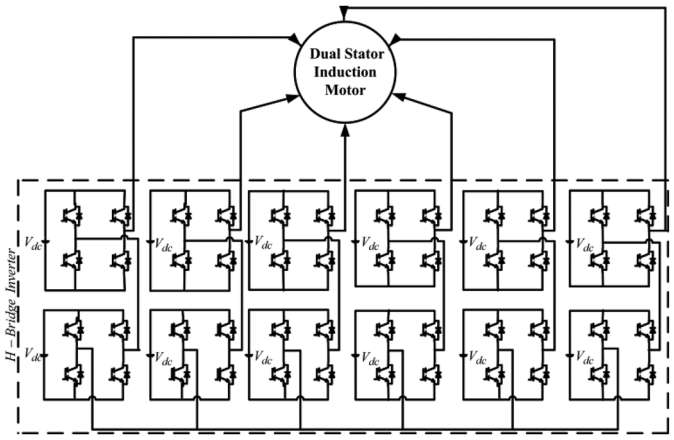

Figure 1. Five-level CHB-MLI connected to DSIM, V_{dc}; DC voltage of inverter cell.

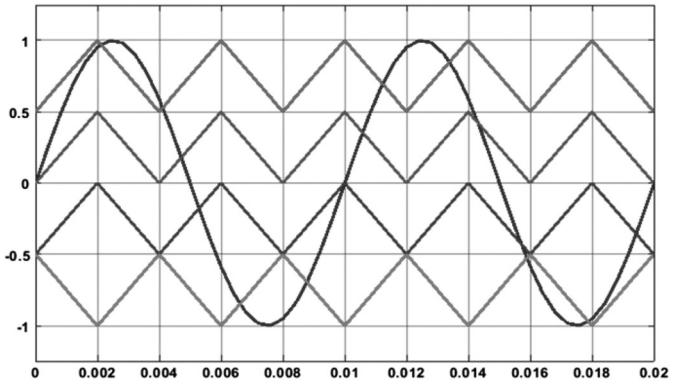

Figure 2. In-phase disposition method.

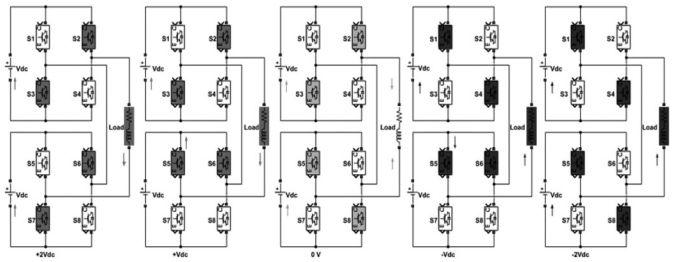

Figure 3. Different stages of output voltage level.

2.2 Proposed In-Phase Disposition

In the in-phase disposition (IPD) modulation scheme, the triangular carriers are so disposed that the upper three carriers are in the same phase, but the lowermost carrier signal is displaced by 180 degrees. The proposed IPD PWM technique waveform is illustrated in Fig. 2, where all triangular carriers are compared with the reference signal for a five-level inverter. CHB-MLI with a single-phase leg with different switching stages of voltage level with ideal insulated gate bi-polar transistor (IGBT) switches is shown in Fig. 3. Each bridge is connected to a separate DC source, generating five voltage levels +2Vdc, +Vdc, 0, -Vdc, and -2Vdc by selecting the different combinations of switches tabulated in Table 1.

Table 1
Switching States for a Five-Level CHB-MLI using IPD Topology

Output	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$+2V_{dc}$	0	1	1	0	0	1	1	0
$+V_{dc}$	0	1	1	0	1	1	0	0
0	0	1	1	0	1	0	0	1
$-V_{dc}$	1	0	0	1	1	1	0	0
$-2V_{dc}$	1	0	0	1	1	0	0	1

Table 2
Parameters and Rating of Six-Phase Induction Motor under Test

Power (P)	1HP	Stator resistance (r_s)	4Ω
Voltage (V)	220 V	Rotor resistance (r_r)	4Ω
Frequency (f)	50 Hertz	Mutual inductance (L_m)	782.7 mH
Reference speed	1,500 rpm	Stator and rotor inductance (L_s, L_r)	808.17 mH
Current	1.801 Amp	Moment of inertia (J)	.0088 Kg-m^2

The output voltages obtained from each H-bridge inverter leg are summed up to obtain five-level stepped voltage by connecting the synthesized leg in series. A five-level cascaded H-bridge inverter has (2l+1) voltages where "l" represents each inverter cell's number of separate DC sources.

3. Results of Simulation

The performance of the CHB five-level inverter using PD, POD, APOD, and IPD topologies are analysed using the symmetrical operating mode of the inverter with DSIM as a load. Matlab/Simulink environment is used to simulate the proposed topologies. The parameters of the motor are tabulated in Table 2. Figure 4. shows the five-level six-phase output, variable frequency, amplitude voltage of CHB-MLI to drive the DSIM. A close-loop volts/Hertz control is used for controlling the drive, considering the modulation index unity.

3.1 Phase Disposition

The five-level output voltage of CHB-MLI using PD topology is shown in Fig. 5(a). From the waveform, it has been observed that the voltage of the inverter has a THD of 7.75%, as shown in Fig. 5(b). The steady-state stator current (I_{s1}) of the DSIM has a THD of 3.02% as shown in Fig. 6.

3.2 Phase Opposition Disposition

Figure 7 shows that the inverter's voltage response has a THD of 8.28% when implemented with POD topologies.

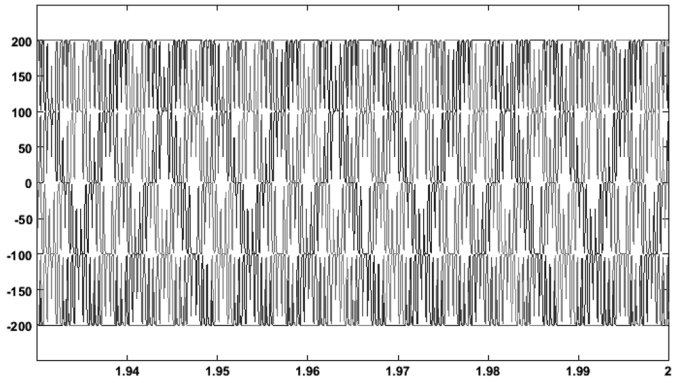

Figure 4. Five-level six-phase output of CHB-MLI.

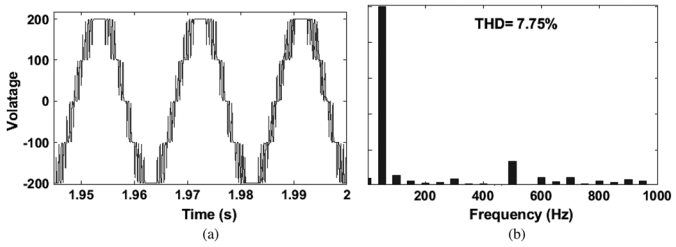

Figure 5. CHB-MLI using PD topology: (a) output voltage and (b) harmonic content.

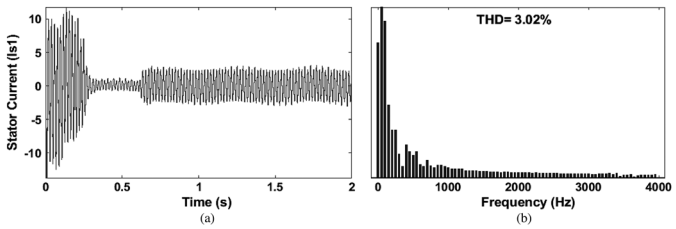

Figure 6. CHB-MLI using PD topology: (a) stator current (I_{s1}) and (b) harmonic profile.

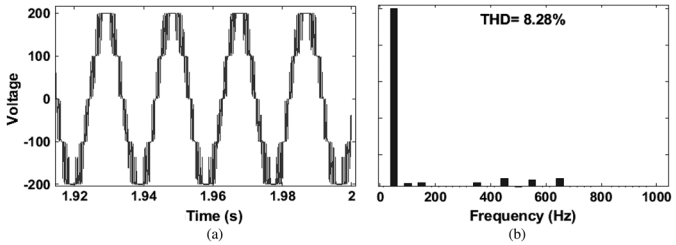

Figure 7. CHB-MLI using POD topology: (a) output voltage and (b) harmonic content.

The motor's steady-state stator current (Is_1) has a fundamental value of 2.605A with a harmonic distortion of 4.99%, as illustrated in Fig. 8.

3.3 Alternate Phase Opposition Disposition

The voltage across the MLI using APOD topology has a THD content of 8.12%, as shown in Fig. 9. In comparison,

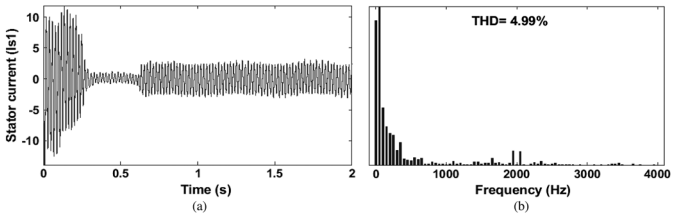

Figure 8. CHB-MLI using POD topology: (a) stator current (I_{s1}) and (b) harmonic content.

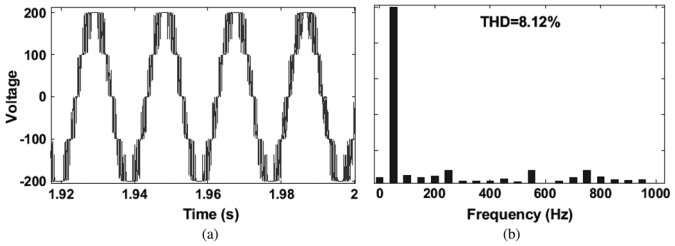

Figure 9. CHB-MLI using APOD topology: (a) output voltage and (b) harmonic content.

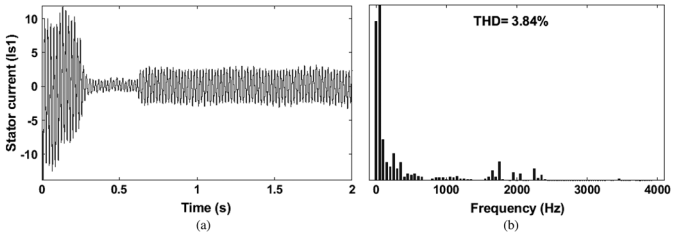

Figure 10. CHB-MLI APOD topology: (a) stator current (I_{s1}) and (b) harmonic content.

the steady-state stator current has a magnitude of 2.615A with a harmonic content of 3.84%, as depicted in Fig. 10.

3.4 In-Phase Opposition Disposition

The drive implemented with the proposed scheme has voltage harmonics of 6.15% and stator current harmonics of 1.7%, as illustrated in Figs. 11 and 12. Simulation results are categorized according to the topologies used to compare the performance of the induction motor drive and are summarized in Table 3. The analysis shows that CHB-MLI when implemented with the proposed scheme results in better performance with low harmonic content in the output waveform of load voltage and current, making the drive suitable for medium- and high-power applications. Table 4 shows the comparative analysis of magnitude and percentage THD of source voltage and current for all the six phases using the topologies mentioned above. The analysis shows that inverter implemented with IPD topology offered minimum THD compared to their counterparts.

4. Real-Time Validation of Simulation Results

OP4500 is a real-time digital simulator that provides a simulation platform for Matlab-based models and simulates

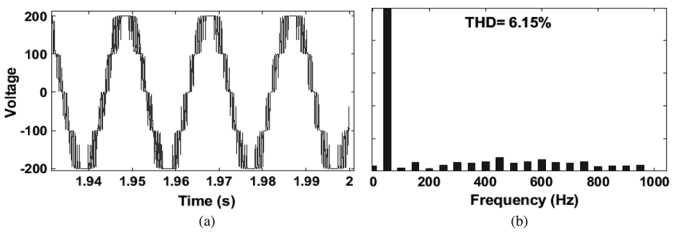

Figure 11. CHB-MLI using IPD topology: (a) output voltage and (b) harmonic content.

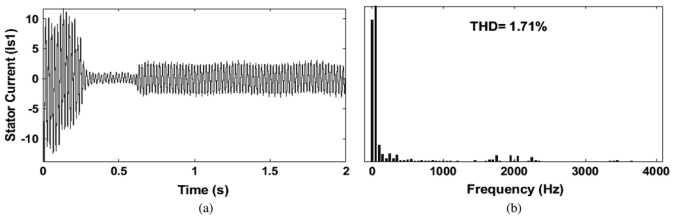

Figure 12. CHB-MLI using IPD topology: (a) stator current (I_{s1}) and (b) harmonic content.

Table 3
Percentage THD using Different Topology

Sr. no.	Topologies	Parameters	THD	Fundamental value
1	PD	Stator current	3.02%	2.457 A
		Voltage across MLI	7.75%	200.16 V
2	POD	Stator current	4.99%	2.605 A
		Voltage across MLI	8.28%	210.6 V
3	APOD	Stator current	3.84%	2.615 A
		Voltage across MLI	8.12%	205.3 V
4	IPD	Stator current	1.70%	2.14 A
		Voltage across MLI	6.15%	198.9 V

at a high-speed rate by using multiple cores. First of all, the Matlab/Simulink platform-based model is simulated in a host computer containing the real-time software connected to the real-time (RT) simulator. Then, its results are recorded by a digital storage oscilloscope Yokogawa DL750, as shown in Fig. 13.

The five-level six-phase output of CHB-MLI using the proposed IPD topology is shown in Fig. 14. The result is measured by keeping the scale down to 1/10. Figure 15 illustrates the six output voltages of the inverter represented by the six channels (CH1–CH6) of the digital oscilloscope using the proposed PWM scheme. It can be seen from the output waveform that the voltages of the channels (CH1–CH5) are in the same phase, and the voltage of the channel (CH6) is in phase opposition which is in good agreement with the proposed topology. Figure 16 shows the real-time current and speed characteristics of the DSIM. It has been observed from the waveform that the drive normally starts

Table 4
Magnitude and Percentage THD of Source Voltage and Current

Sr. no.	Topologies	Parameters	Phase number					
			1	2	3	4	5	6
1	PD	Mag. of source voltage (V)	199.7	199.8	199.7	199.6	199.7	199.8
		% THD of source voltage	2.2	2.3	2.2	2.1	2.2	2.3
		Mag. of source current (A)	2.51	2.50	2.49	2.50	2.49	2.51
		% THD of source current	2.58	2.55	2.56	2.55	2.56	2.58
2	POD	Mag. of source voltage(V)	200	199.9	199.7	199.9	199.8	199.8
		% THD of source voltage	3.4	3.3	3.1	3.3	3.2	3.2
		Mag. of source current (A)	2.59	2.58	2.57	2.58	2.57	2.58
		% THD of source current	3.01	3.00	2.59	3.00	2.57	3.00
3	APOD	Mag. of source voltage(V)	200	200.1	200.2	200.1	200	200.1
		% THD of source voltage	3.0	3.1	3.2	3.1	3.0	3.1
		Mag. of source current (A)	2.55	2.57	2.58	2.57	2.55	2.57
		% THD of source current	2.98	2.99	3.01	2.99	2.98	2.99
4	IPD	Mag. of source voltage (V)	199.9	200	199.8	199.9	200	200
		% THD of source voltage	2.45	2.48	2.44	2.45	2.48	2.48
		Mag. of source current (A)	2.23	2.25	2.22	2.23	2.25	2.25
		% THD of source current	1.00	1.01	.99	1.00	1.01	1.01

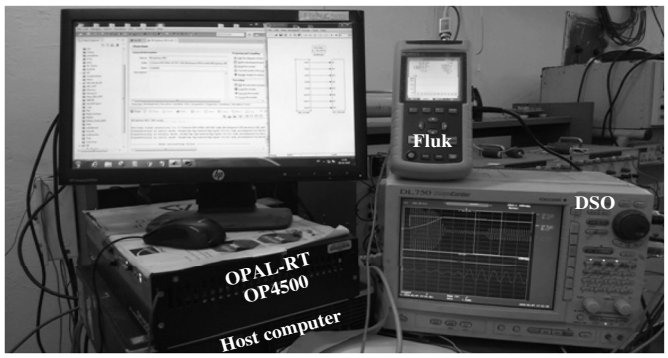

Figure 13. Lab set-up of Opal-RT.

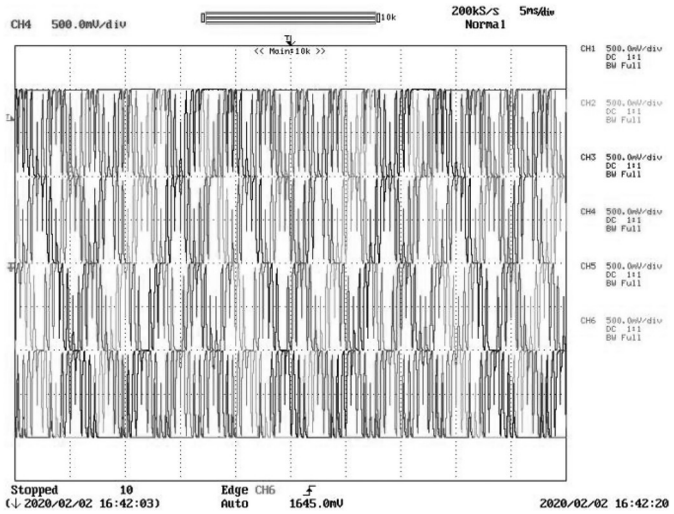

Figure 14. Real-time five-level six-phase output of CHB-MLI using IPD topology.

under a no-load condition. As the drive's speed increases toward the reference speed of 1,500 rpm, a load torque of 4 N.m at an instant 0.6 s is applied, which reduces the drive's speed to 1,499 rpm, and speed reaches a steady state. The good control of drives speed shows the proper implementation of the control technique. Figure 17 shows the real-time torque characteristic of CHB-MLI-fed DSIM drive. It is observed that when the drive is implemented with the proposed topology, the torque ripple is reduced. Channel (CH1) shows the electromagnetic torque (T_e), whereas channel (CH2) represents the mechanical torque (T_m). Also, channel (CH3) represents the steady-state stator current (Is1) variation as a function of load torque. Figure 18 illustrates that the stator current has a THD of 1.7% by implementing the proposed topology within the IEEE standard limit.

Finally, the proposed IPD inverter-based drive is compared with PD-, POD-, and APOD-based drive. In particular, power loss and efficiency are used to compare the different topologies. Here, output frequency of the inverter is 50Hz, and the sampling frequency is 5 kHz.

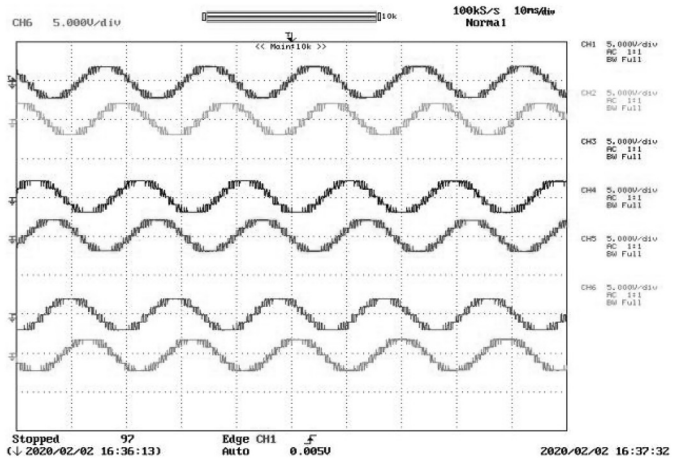

Figure 15. Real-time six-phase voltage of CHB-MLI-fed DSIM using IPD topology.

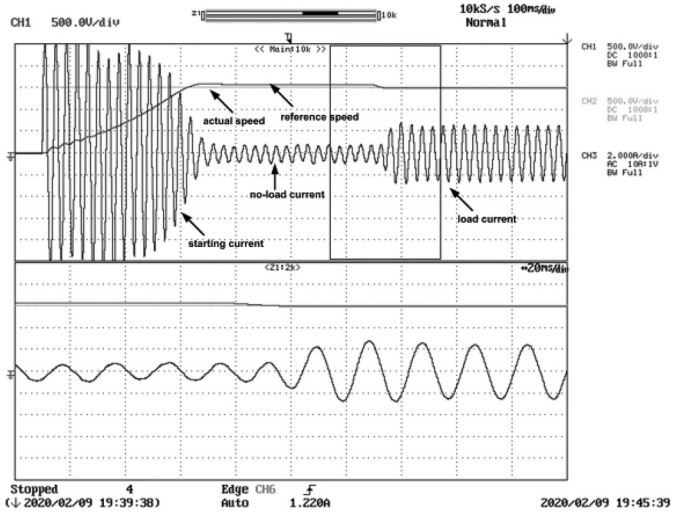

Figure 16. Real-time speed and current waveform of CHB-MLI-fed DSIM using IPD topology.

Figure 19 compares the performance efficiency evaluation of proposed techniques with other aforementioned techniques. It is observed from the curve that the proposed topologies have higher efficiency at different load torque operations. Table 5 compares the efficiency of the DSIM drive using the different PWM techniques. Switching and conduction losses are the main two losses in the drives. The switching losses are determined when the device is turned ON or OFF, total commutation time, and by the current and voltages across the device during the operation [20]. At the same time, the conduction losses are determined by the instantaneous current passing through the machine and the saturation voltage of the device. Here, through simulation, input power and output power are measured to calculate the efficiency, and average current and saturation voltage of the device are measured to calculate the conduction losses. From the calculation, it was observed that conduction losses are higher than the switching losses. However, the losses of different techniques are almost equal,

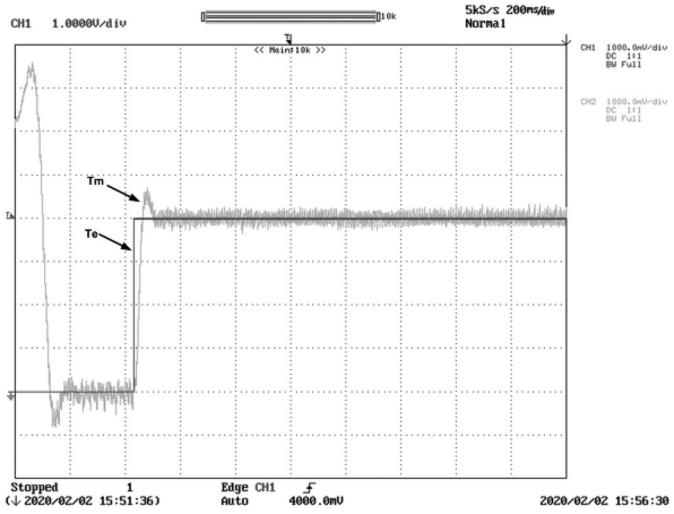

Figure 17. Real-time torque profile of CHB-MLI-fed DSIM using IPD topology.

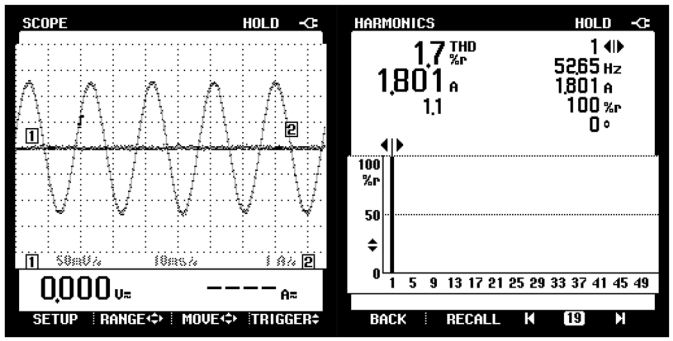

Figure 18. Stator current THD profile of CHB-MLI using IPD topology.

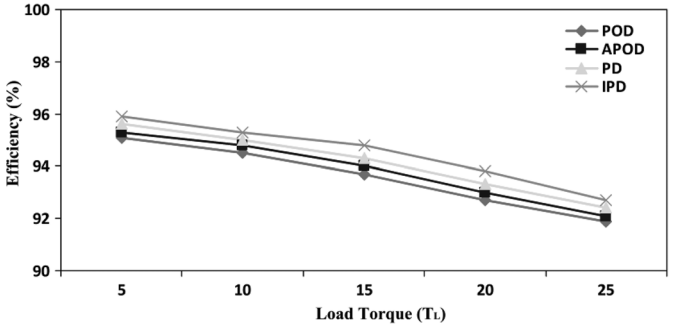

Figure 19. Comparative efficiency analysis using different topologies.

so the efficiency of the drive is nearly the same still IPD approach offers higher efficiency.

It is very difficult to make any genuine cost comparison among competitive topologies, as components' cost varies from country to country. However, voltage and power handling capacity of the reported topologies also varies from authors to authors. Therefore, it would be quite unfair to allocate the same price for the switches with different voltage pressures [21]. However, the article we

Table 5
Comparison of Power Loss and Efficiency using PD, POD, APOD, and IPD Topologies

Input Power	Power loss (W)				Efficiency (%)			
(W)	PD	POD	APOD	IPD	PD	POD	APOD	IPD
175.9	18.2	19.8	19.3	16.2	92.6	92.1	92.4	92.9
193.1	21.5	23.7	22.9	19.2	93.5	92.8	93.1	93.8
229.9	25.2	26.7	26.1	23.5	94.3	93.9	94.0	94.9
292.7	26.8	28.7	27.7	24.7	95.1	94.7	95.2	95.6
330.2	30.5	32.1	31.2	28.8	95.9	95.1	95.7	96.1

Table 6
Comparison of Five-Level Topologies with the Existing Topologies

Parameters	FC	NPC	[22]	[23]	[24]	[25]	Proposed CHB-MLI
No. of diodes	0	12	0	0	2	2	0
No. of gate drivers	8	8	22	20	7	6	8
No. of switches	8	8	22	20	7	6	8
No. of DC sources	4	4	1	4	2	1	2
No. of capacitors	6	0	8	0	0	2	0
No. of bidirectional switches	0	0	0	0	1	1	0
Total cost	81.97	65.89	177.92	121.20	51.09	62.37	48.13
Total blocking voltage in per unit	12	12	22	20	8.5	9	12

submitted is critically compared for their international price in USD. Table 6 also compares IPD topology with other existing topologies in terms of numbers of diodes, drivers, switches, DC sources, capacitors, and bidirectional switches, and total cost.

5. Conclusion

A new IPD PWM technique is used to control switches of five-level CHB-MLI, which influence current and voltage harmonic content. The proposed work aims to compare the performance of a new IPD topology based on CHB-MLI with different multicarrier PWM topologies which are used to drive DSIM. OPAL-RT (OP4500) is used to validate the proposed modulation technique. The analysis of results shows that the proposed topology mitigates the current and voltage harmonics to 1.7% and 6.15%, respectively, and increases the system's efficiency with reduced power loss and torque ripple with consistent drive performance over the entire speed range.

References

[1] G.K. Singh, Multi-phase induction machine drive research-A survey, *Electric Power Systems Research*, *61*(2), 2002, 139–147.

[2] J. Apsley, S. Williamson, A. Smith, and M. Barnes, Induction motor performance as a function of phase number, *Proceedings of the Institution of Electrical Engineers-Electric Power Applications*, *153*(6), 2006, 898–904.

[3] J.S. Thongam, M. Tarbouchi, A. F. Okou, D. Bouchard, and R. Beguenane, Trends in naval ship propulsion drive motor technology, *Proc. IEEE Elect. Power Energy Conf.*, 21–23, 2013, 1–5.

[4] R.V. Nair, *et al.*, Stacked multilevel inverter fed six phase induction motor with reduced DC link and lower voltage devices, *IEEE International Conference on Industrial Technology (ICIT)*, 2017, 342–347.

[5] H. Belkamel, *et al.*, Novel three-phase asymmetrical cascaded multilevel voltage source inverter, *IET Power Electronics*, *6*(8), 2013, 1696–1706.

[6] D.Kumar, R. Akhil Raj, R.K. Nema, and S. Nema, A novel higher level symmetrical and asymmetrical multilevel inverter for solar energy environment, *IETE Journal of Research*, 2020, 1–13.

[7] K.A. Chinmaya and G.K. Singh, Experimental analysis of various space vector pulse width modulation (SVPWM) techniques for dual three-phase induction motor drive, *International Transactions on Electrical Energy Systems*, *29*(1), 2019, e2678.

[8] V. Rathore and K.B. Yadav, Analytical model based performance characteristics analysis of six-phase induction motor, *Proceedings of the International Conference on Advances in Electronics, Electrical & Computational Intelligence (ICAEEC)*, 2019 Apr 14; Available at SSRN 3575381.

[9] K. Deepa, *et al.*, A study of comparative analysis of different PWM techniques, *International Conference On Smart Technologies For Smart Nation (Smart. Tech. Con.)* (Bangalore: IEEE, 2017), 1144–1149.

[10] R.K. Ahuja and A. Kumar, MATLAB simulation and analysis of nine-level inverter using different schemes of sinusoidal PWM, *International Journal of Innovative Research in Science, Eng and Tech*, *3*(6), 2014, 13626–13633.

[11] V. Rathore, K.B. Yadav, and S. Dhamudia, An implementation of nine-level Hybrid Cascade Multi-level Inverter (HCMLI) using IPD-topology for harmonic reduction, in *Nanoelectronics, Circuits and Communication Systems* (2020), 203–210.

[12] J. Rodriguez, J.S. Lai, and F.Z. Peng, Multilevel inverters: A survey of topologies, controls, and applications, *IEEE Transactions on Industrial Electronics*, *49*(4), 2002, 724–738.

[13] M. Malinowski, K. Gopakumar, J. Rodriguez, and M.A. Perez, A survey on cascaded multilevel inverters, *IEEE Transactions on Industrial Electronics*, *57*(7), 2009, 2197–2206.

[14] Aldo Boglietti, *et al.*, Efficiency analysis of PWM inverter fed three-phase and dual three-phase high frequency induction machines for low/medium power applications, *IEEE Transactions on Industrial Electronics*, *55*(5), 2008, 2015–2023.

[15] B. Lyas, *et al.*, Multilevel SVM for six-phase multilevel inverters to drive dual stator induction machine, *International Journal of Power and Energy Systems*, *40*(2), 2020.

[16] O.E. Youssef, A new open-loop volts/Hertz control method for induction motors, *Twentieth International Middle East Power Systems Conference (MEPCON)* (IEEE, 2018), 266–270.

[17] A. Elnady and M.S. Suleiman, Simulation and experimental comparison between multilevel and conventional inverters, *International Journal of Power and Energy Systems*, *37*(3), 2017.

[18] J. Tandekar, A. Ojha, and S. Jain, Five-level cascaded H-bridge MLC-based shunt active power filter for active harmonics mitigation in distributed network, *Journal of Circuits, Systems and Computers*, *28*(02), 2019, 1950035.

[19] K. Janardhan, A. Mittal, and A. Ojha, A symmetrical multilevel inverter topology with minimal switch count and total harmonic distortion, *Journal of Circuits, Systems and Computers*, *29*(11), 2019, 2050174.

[20] V. Rathore and K.B. Yadav, Comparative efficiency analysis of five-level dual three-phase multilevel inverter fed six-phase induction motor drive, *International Journal of Numerical Modelling*, *35*(3), 2021, e2981.

[21] D. Kumar, R.K. Nema, and S. Gupta, Development of fault-tolerant reduced device version with switched-capacitor based multilevel inverter topologies, *International Transactions on Electrical Energy Systems*, *31*(7), 2021, e12893.

[22] A. Chen, L. Hu, L. Chen, Y. Deng, and X. He, A multilevel converter topology with fault-tolerant ability, *IEEE Transactions on Power Electronics*, *20*(2), 2005, 405–415.

[23] J. Nicolas-Apruzzese, S. Busquets-Monge, J. Bordonau, S. Alepuz, and A. Calle-Prado, Analysis of the fault-tolerance capacity of the multilevel active-clamped converter, *IEEE Transactions on Industrial Electronics*, *60*(11), 2012, 4773–4783.

[24] K. Sivakumar, A fault-tolerant single-phase five-level inverter for grid-independent PV systems, *IEEE Transactions on Industrial Electronics*, *62*(12), 2015, 7569–7577.

[25] S.P. Gautam, S. Gupta, and L. Kumar, Reliability improvement of transistor clamped H-bridge-based cascaded multilevel inverter, *IET Power Electronics*, *10*(7), 2017, 770–781.

Biographies

Vishal Rathore received his B.E. degree in Electrical and Electronics Engineering from Laxmi Narayan College of Technology (LNCT), Bhopal, India, in 2007, M.Tech in Electrical Drives from Maulana Azad National Institute of Technology (MANIT), Bhopal, India, in 2012. Currently, he is working towards his PhD degree at NIT Jamshedpur, Jharkhand, India. His fields of interest include Multilevel Inverters based Multiphase Drives, Real-time controllers for power electronics based drives systems, and usage of power electronics in transit systems.

K. B. Yadav received his B.Sc. in Electrical Engineering from Regional Institute of Technology presently National Institute of Technology Jamshedpur, India, in 1989, M.Sc. in power electronics and PhD from Indian Institute of Technology Roorkee, India, in 2007. Currently, he is an Associate Professor in the Department of Electrical Engineering at the National Institute of Technology Jamshedpur, India. His fields of interest include Multiphase Electrical Machines, Power Electronics & Electric Drives, Power System Economics, Renewable power generation and Smart Grid.